Control and Protection Strategies for a Universal Power Quality SMES Compensator

Diego Raggini
RSE S.p.A.
Milano, Italy
diego.raggini@rse-web.it

Riccardo Chiumeo
RSE S.p.A.
Milano, Italy
riccardo.chiumeo@rse-web.it

Alessio Clerici
RSE S.p.A.
Milano, Italy
alessio.clerici@rse-web.it

Chiara Gandolfi
RSE S.p.A.
Milano, Italy
chiara.gandolfi@rse-web.it

Daniele Gargantini
RSE S.p.A.
Milano, Italy
(*at present at Dimac Red S.p.A*)
d.gargantini@dimacred.com

***Abstract*—The paper describes the control and protection strategies of a device conceived to improve Power Quality in Low Voltage (LV) electrical distribution grid. The device, studied in the frame of the research project "DRYSMES4GRID", acts as an active filter, compensating load harmonics and network disturbances (voltage dips and micro-interruptions) thanks to a Superconducting Magnetic Energy Storage system (SMES).**

The control logics are presented with a particular focus on detecting and overcoming overload or internal and external fault condition. The effectiveness of the proposed control strategies has been investigated in ATPdraw simulation environment, using a detailed network and device model.

Keywords—SMES; Power Quality; Power Electronics.

I. INTRODUCTION

The continuous progress of the electronics devices has brought to a distorting loads relevant increment. These types of devices are disturbances generators but at the same time are sensitive loads to a low quality level of the electric distribution network [1]. The study of new solutions to improve the Power Quality (PQ) of the electric grids has a relevant position in the research field, especially the analysis of power electronics devices for the protection of sensitive loads.

DRYSMES4GRID is a research project financed by the Italian Ministry of Economic and Development and sees the participation of different Italian partners (RSE SpA, ASG SpA, University of Bologna, ICAS and CNR-SPIN) http://www.drysmes4grid.spin.cnr.it/. The aim of the project is to demonstrate the feasibility of a cost-competitive Superconductive Magnetic Storage System (SMES) based on MgB2 with a cryogen free cooling system.

The Universal Power Compensator (UPC) has been presented as a suitable power electronic device to interconnect the SMES to the low voltage (LV) distribution grid for protecting sensitive loads [2-3]. This paper, which is the synthesis of a previous work [4] elaborated in RSE S.p.A., presents the new features implemented in the control system of the compensator to protect the device against faults and overloads. In section II, the Universal Power Compensator is presented, paying attention to the control strategies. Two current limitations strategies, implemented for the device protection during overload conditions, are described in Section III, as well as the simulative analysis to verify their performances. Section IV outlines the internal faults detection logic and how these conditions are managed by the compensator. Finally, conclusions are drawn in Section V.

II. UNIVERSAL POWER QUALITY SMES COMPENSATOR

The analysis object of this paper is the universal Power Quality compensator [5-6], connected in the LV distribution grid near disturbing/sensitive loads, acting:

- grid connected as an active filter, able to compensate distorted unbalanced load currents, fast active and reactive power fluctuations (peak shaving);
- islanding, after a grid fault detection, as an UPS (Uninterruptable Power Supply) able to supply sensitive loads using the storage systems (SMES), connected in its DC section.

Fig. 1 shows the scheme of the designed system, made by:

- the interface device: an inverter with its commutation inductances, filters, coupling transformer and static switch;
- the SMES: an inductance L_{SMES} and a DC/DC chopper.

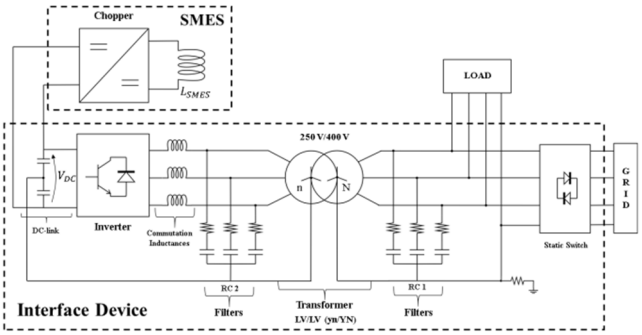

Fig. 1 SMES and Interface device scheme

In Table I the main design parameters are presented.

978-8-8872-3747-4©2020 AEIT

TABLE I. MAIN CHARACTERISTICS DESIGN OF THE DEVICE

Quantities	Symbol	Inverter	Chopper (I/V)
Rated Power	A_n	200 kVA	200 kW
DC Voltage	V_{DC}	750 V	
AC Voltage	V_{AC}	250 V	
DC Capacitor	C_{DC}	81 mF	
Commutation Frequency	f_{sw}	12.6 kHz	5 kHz
Maximum current	I_{max}	1640 A	400 A
Minimum current	I_{min}		135 A
Coil inductance	L_{SMES}		4.33 H
Commutation Inductance	L_{Com}	16.50% A_N	
Transformer Resistance	R_{tr}	3.5% A_N	
Transformer Inductance	L_{tr}	3.5% A_N	
RC filter Capacitor 2	C_{f2}	0.50% A_N	
RC filter Resistance 2	R_{f2}	0.50% A_N	
RC filter Capacitor 1	C_{f1}	10.30% A_N	
RC filter Resistance 1	R_{f1}	10.30% A_N	

A. Grid connected and Islanding mode control strategies

Fig.2 shows the generalized blocks scheme, which synthetizes the structure of the current and voltage control loops implemented both for the compensation and island mode.

In order to analyse the compensation performances, both open loop and close loop logics were implemented and tested for the current control strategies.

The main difference between the two controls is that the "open loop" carries out the compensation measuring the load currents while the "close loop" the grid currents.

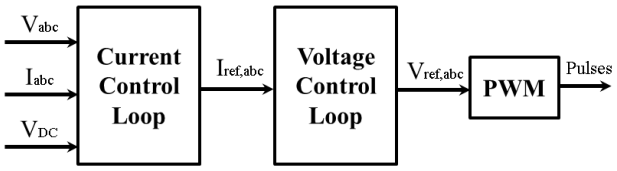

Fig. 2 General blocks scheme of the control system

The target of the control strategies is the compensation of all the load reactive power (Q) and the load active power fast variations (P). In this way distorted and unbalanced load currents are compensated and the electric grid has to supply:

- the average value of load active power;
- the active power required to keep constant the voltage on the DC side.

The harmonic selectivity is the suitable solution to avoid the resonance effects of capacitive load. The analysis [5] demonstrates that the close loop without harmonic selectivity is the most suitable for the compensator. In Table II, the control types and their characteristic are summarized and compared.

TABLE II. CONTROL STRATEGIES RECAP

Control Type	Harmonic Selectivity	Current Measured	Reference System	Characteristics
Open Loop	no	Load side	"abc" axes	Compensation of the load P,Q fast variations
Open Loop	no	Load side	Rotating axes "dq"	Compensation of the load P,Q fast variations
Close Loop	yes	Grid side	"abc" axes	Compensation of the load P,Q slow variations
Close Loop	yes	Grid side	"abc" axes	Compensation of the load P,Q fast variations

The island mode control strategy is based on the block scheme of Fig. 2.

In islanding conditions the device provides all the load energy request thanks to the SMES, acting as a UPS.

The control system monitors the grid three-phase voltages, upstream the static switch connection node: when just one rms voltage value decreases below the 90% of the rated value, during a grid voltage disturbance occurrence, the compensator trips the static switch to disconnect the grid and the island operation mode starts.

The software simulations demonstrate that the load voltages have a Total Harmonic Distortion (THD) factor lower than the 8%[1].

When grid steady state conditions are restored, after a delay of 100 ms, grid re-synchronization starts: when the procedure is completed the static switch is closed and the on grid operation is restored with the same compensation tasks before the disturbance occurrence.

III. CURRENT LIMITATION STRATEGY

The inverter has low thermal inertia, when the current reaches value higher than the nominal one it is necessary to impose current limits to avoid semiconductors damages[7-8]. Two current limitations were implemented in the compensator control: an instantaneous current limitation and a "slow" current limitation.

A. Instantaneous current limitation

The instantaneous current limitation is a hardware current limitation strategy and acts directly on the on/off pulses of the valves (Fig. 3). The current limiting threshold has been defined to the maximum commutable current of 1640 A, which is 2.5 times the peak of the nominal current. The rated current (I_n) is:

$$I_n = \frac{A_n}{V_{AC} \cdot \sqrt{3}} = 464 \text{ A} \quad (1)$$

The instantaneous limitation algorithm operates the valve switch off where the limiting threshold is exceeded in one direction, without closing the complementary valve; if the valve to be operated is already open, no action shall be taken. Once switched off, the valve remains open until the

[1] This value is in compliance with the standard CEI EN 50160:2011, "Qualità del servizio elettrico".

PWM modulator sends a new firing command. Once this command is executed, the regular switching of the valves "from PWM" is restored, until an overcurrent occurs again such as to determine a new limitation logic action.

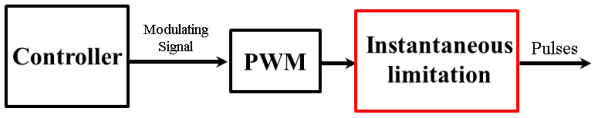

Fig. 3 Control scheme of the instantaneous current limitation

The effectiveness of the instantaneous limitation action has been tested, simulating a balanced three-phase overload. The power absorption of the load is twice the nominal value of the compensator (200 kVA). Fig 4 shows the three-phase currents supplied by the inverter in islanding: at 0.3 s the load is connected, the currents reach both the positive and negative thresholds (± 1640 A), highlighting the "peak cuts" of the sinewave due to the limitation algorithm. In Fig. 4 it is also zoomed the detail of the limitation effect on one phase current, with the ripple frequency increment.

In general, the instantaneous limitation is suitable to limit quickly the overcurrent but only for short periods (e.g. 100 ms), due to the stresses to which the inverter valves and the components of the device are subjected during this operating condition.

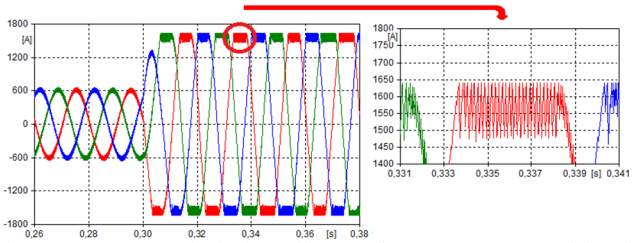

Fig. 4 Instantaneous limitation effect on the currents generated by the inverter

The instantaneous limitation strategy modifies the commutation timing, causing a significant harmonic distortion growth on load voltages.

Considering the previous balanced three-phase overload, during the island mode (Fig. 5), the load voltage waveforms are significantly distorted, while on grid mode (Fig. 6), where voltages are "imposed" by the grid itself, the same voltages are less distorted.

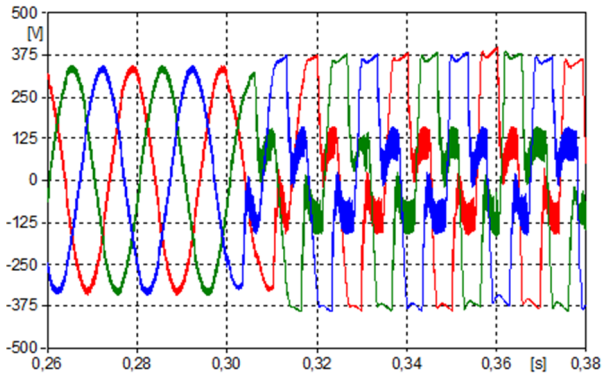

Fig. 5 Three-phase voltage trend on the load during the island mode for the instantaneous current limitation

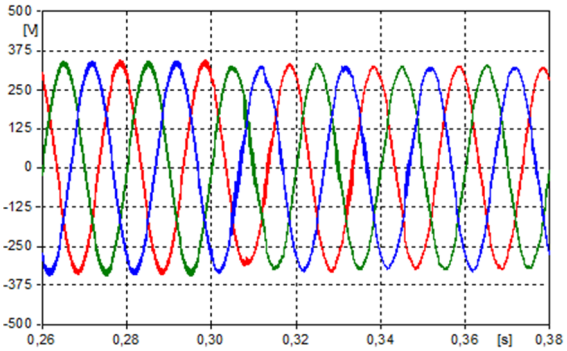

Fig. 6 Three-phase voltage trend on the load during the compensation mode for the instantaneous current limitation

Table III shows the comparison of the load voltage THD during the grid connection and islanding, with or without the presence of the instantaneous limitation. As shown in the voltage load trend, the THD comparison confirms the high harmonics presence. This condition happens in rare situations (fault, overloads) to protect the integrity of the inverter, that is operating over its capability.

TABLE III. VOLTAGE THD FOR A BALANCED THREE-PHASE LOAD

Operation Mode	**Without** instantaneous limitation	**With** instantaneous limitation
Grid connected	0,19%	1,61%
Island	0,66%	69,77%

B. Slow Current Limitation

To overcome THD issues given by instantaneous limitation, a slow current limitation has been developed; it is a software algorithm control, which generates limited sinusoidal currents. As a result, the slow limitation acts after the fast limitation and it can operate for the long periods. The limiting current threshold defines the maximum rms current (I_{MAX}) generated by the compensator, fixed at 1.5 times the rated value of the current I_n (700 A).

Each phase current is regulated by the limitation control logic presented in Fig. 7, allow to manage unbalanced overloads.

The algorithm (Fig. 7) calculates the variable "outis" and limits the phase current proportionally by multiplying the modulation signal. Starting from the difference between the threshold limiting value and the rms phase current ("eps"), the variable "outis" is obtained as output of the "Non-linear" block of Fig. 7 in respect to the following conditions:

$$\begin{cases} \text{eps} > 100, & \text{outis} = 1 \\ 0 < \text{eps} \geq 100, & \text{outis} = \text{outis}_{\min} + \left(\dfrac{1-\text{outis}_{\min}}{\text{eps}^*}\right) * \text{eps} \\ \text{eps} \leq 0, & \text{outis} = \text{outis}_{\min} \end{cases} \quad (2)$$

Where eps^* has been fixed to 100 A, which means that the limitation control is activated when the inverter current is:

$$I_{MAX} - \text{eps}^* = 600 \text{ A} \quad (3)$$

"Outis" is filtered to avoid that the mesurement current oscillations can affect the modulating signals and, consequently, disturb the voltage generation.

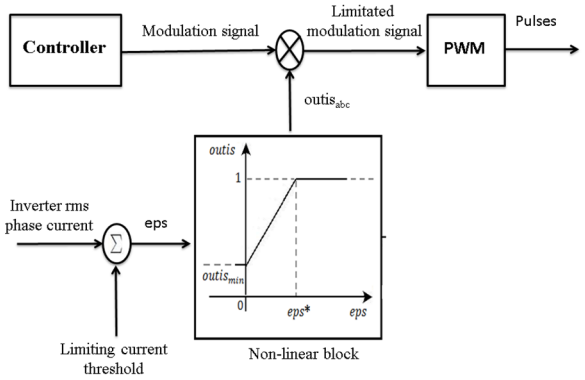

Fig. 7 Slow current limitation block scheme

The limitation performances have been tested by simulating a single-phase overload on the phase "a" at 0.3 s, lasting 400 ms during the island mode. Fig. 8 shows inverter three-phase currents: at 0.3 s the instantaneous limitation effect is highlighted (phase current limited between ± 1640 A) till the slow current limitation starts to operate (at 0.45 s). When the overload is over, the current reaches the steady-state values after a transition of 50 ms, due to the voltage and current regulator dynamic.

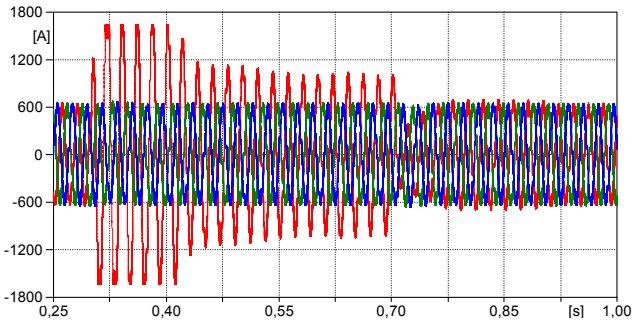

Fig. 8 Three-phase currents signals generated by the inverter during a single-phase overload in island mode

During the overload, the modulating signal of the phases "b" and "c" do not vary because of the decouple action of the slow limitation algorithm for each phase (Fig. 9). The modulating signal for the phase "a" decreases its value to limit the current. At 0.7 s, "outis" for the phase "a" (light-blue signal in Fig. 9), takes 300 ms to reach the unit value, because of the delay introduced by the "outis" filtering.

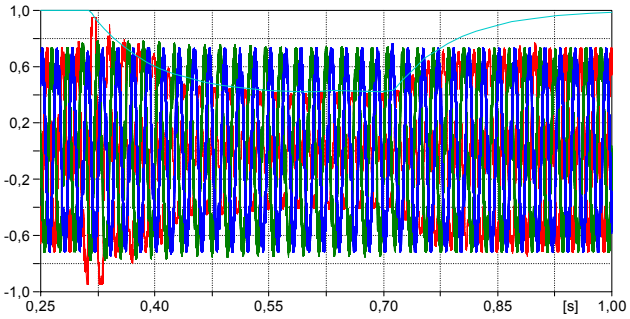

Fig. 9 Three-phase modulating signals (red,blu,green) and "outis" signal for phase "a", during a single-phase overload in island mode.

The phase "a" load voltage (Fig. 10) is distorted (instantaneous current limitation effect) for 100 ms, then it decreases as a necessary consequence of the slow limitation action, keeping the sinusoidal waveform thanks to a precaution on the voltage regulator [9].

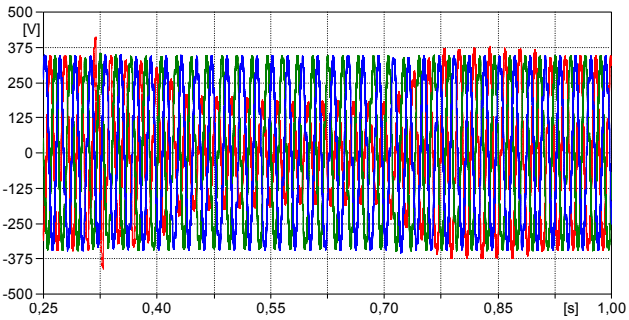

Fig. 10 Three-phase voltage signals measured on the load during a single-phase overload in island mode

IV. FAULTS DETECTION AND MANAGMENT

The universal power compensator design requires an adequate protection against the faults that potentially could affect its electric components. The analysis identifies two faults categories: the external and the internal faults to the compensator.

The external faults could happen at load side or at grid side. The load has its own protection devices so in case of fault the compensator is not affected by disturbances. If a fault happens at the grid side and causes a voltage dip higher than the 10% of the nominal value, the compensator recognizes the voltage dip and enters in island mode, protecting the sensitive load.

The internal faults could happen in the portion of the compensator electric scheme included in the yellow rectangle in Fig. 11. The control system of the compensator must detect and manage the internal fault.

A. Residual current relay

A residual current device has been chosen to detect phase-ground, phase-neutral and phase-phase "internal faults", while it does not recognize the external fault.

The device acquires, as inputs, the measurements of the following currents (Fig. 11):

- inverter currents (I_{inv});
- grid side filters currents (I_C);
- load currents (I_{load});
- grid fed currents (I_{grid}).

The device algorithm calculates the vector sum of the input currents for each measured phase. The result is equal to the opposite current of the internal fault current (I_{fault}):

$$I_{inv} + I_C + I_{load} + I_{grid} + I_{fault} = 0$$

$$I_{inv} + I_C + I_{load} + I_{grid} = -I_{fault} \quad (4)$$

Allowing the internal fault detection during its occurrence.

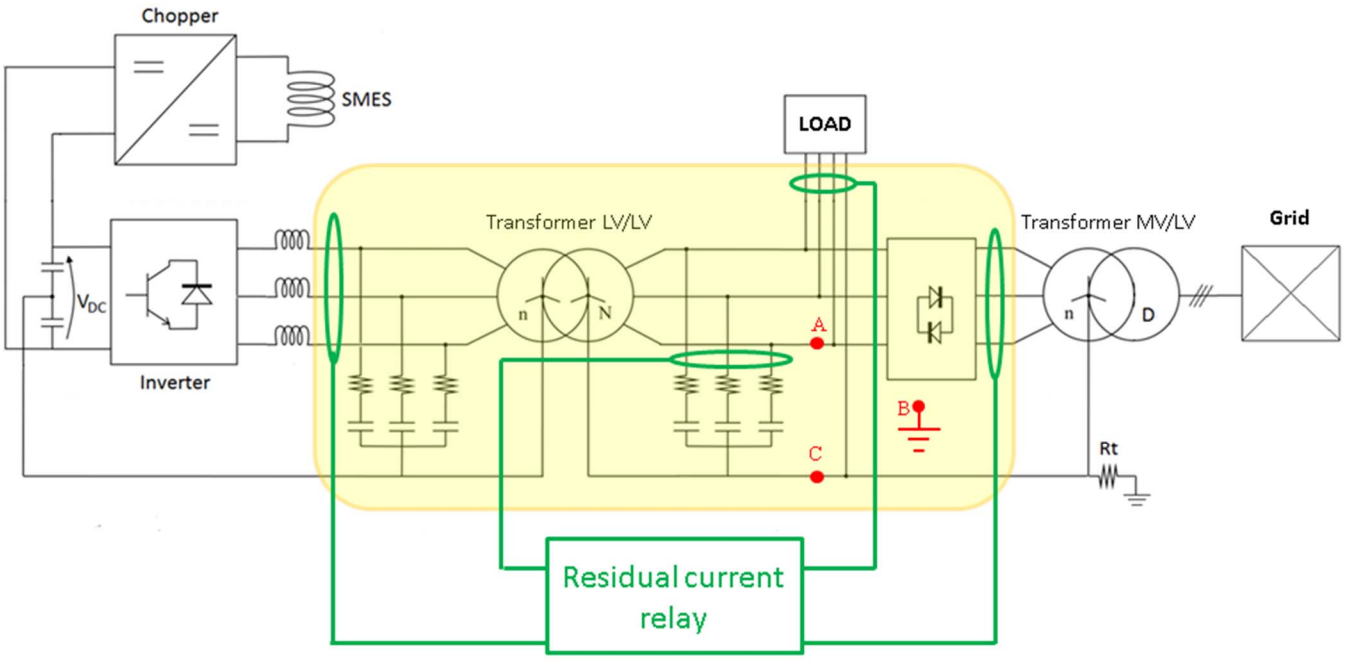

Fig. 11 Residual current relay

In order to test the response of the relay, two faults have been simulated: single phase-ground and single phase-neutral.

B. Single phase-ground fault

At 0.3 s, the internal fault is simulated between one phase and the ground (point A and B in Fig. 11) in parallel to the load, with a ground resistance (R_g) of 0.1 Ω. The fault current (I_{fault}) flows from the phase to the ground through the ground resistance and the star point resistance (R_t=0.3 Ω) of the LV/LV transformer.

The voltage of the phase "c" affected by the fault on the grid side (green line in Fig. 12) decreases significantly reaching the voltage drop across the fault resistance ($R_g \cdot I_{fault}$).

The fault current flows through the ground resistance of the transformer (R_t), setting a new potential value between the ground and the neutral (before the fault the voltage of the neutral was equal to the ground). As a consequence, the values of the other two phases "a" and "b" (red and blue lines in Fig. 12) increase and their values are given by the sum of the phase-neutral voltage plus the voltage drop across R_t.The phase-neutral voltages do not change.

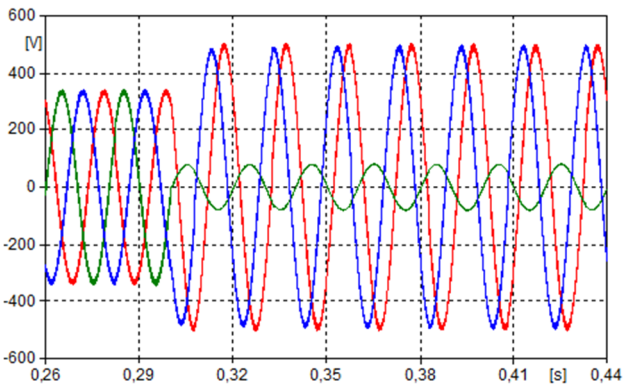

Fig. 12 Phase-ground voltages trend, during the single phase-ground fault

Fig. 13 shows the residual current detected by the relay, in particular it is highlighted the rms current value (brown line) which is acceptable to allow the definition of a protection current threshold.

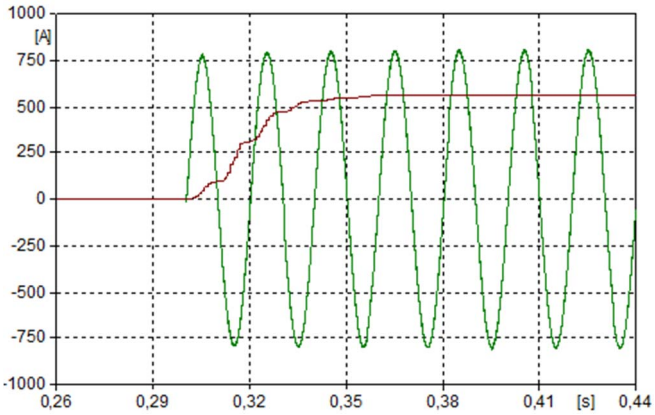

Fig. 13 Residual current trend (green line) and its rms, during the single phase-ground fault

C. Single phase-neutral fault

A second type of internal fault has been simulated between the phase "c" and the neutral (point A and C in Fig. 11) in parallel to the load, with a fault resistance (R_f) of 0.1 Ω. The fault current flows from the phase to the neutral through two different paths: one is the load, and the other one is the star-point of the LV/LV transformer.

At 0.3 s, due to the fault, the phase-neutral voltages values decrease under 10% of the rated value; the control system detects the voltage dip and starts islanding operation. On the load side, the phase-neutral voltages are generated by the inverter, in particular the voltage of phase "b" (green line in Fig. 14) is lower than the other two phase voltages, because of low fault resistance (R_f) value. At the fault occurrence, entering in island mode, the phase-neutral voltages (Fig. 14) and the phase currents (Fig. 15) show the characteristic "peak cuts" of the instantaneous current

limitation action. In this case, during the island mode, the target of the compensator is to provide suitable voltages in order to guarantee he protection device tripping.

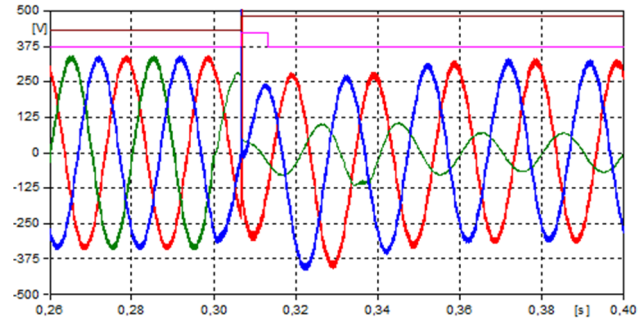

Fig. 14 Phase-neutral voltages trend on the load side and signals of voltage dip detection (pink line) and of disconnection form the main grid (brown line)

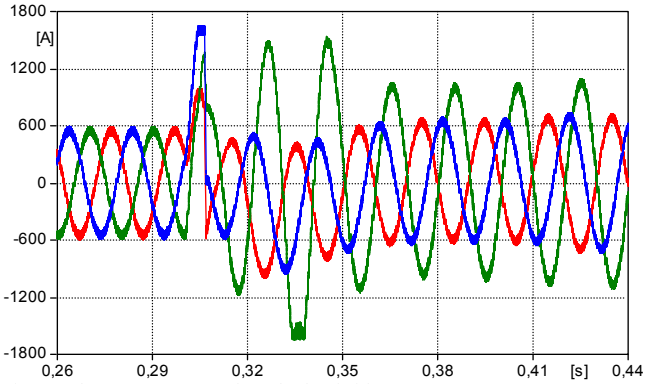

Fig. 15 Phase currents trend on the load side

In the initial instant of the fault, the residual current, detected by the relay (red line in Fig. 16), reaches high value because of the grid contribution. In islanding, I_{fault} is reduced by the instantaneous current limitation of the inverter, the rms current value (50 A) reached in 50 ms, is considered sufficiently high to permit the definition of a protection threshold.

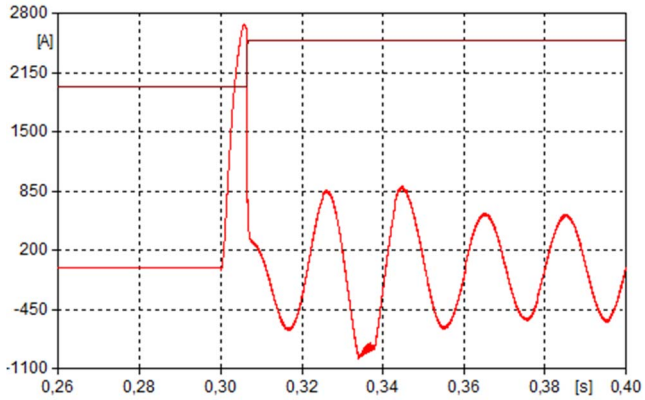

Fig. 16 Residual current (red line), during the single-phase neutral fault and grid disconnection signal (brown line)

V. Conclusion

The limitation logics and the protection strategies have been presented with simulative analysis to demonstrate their feasibility for a universal Power Quality compensator connected to the LV distribution grid, characterized by a SMES. This paper is developed in the frame of the project DRYSMES4GRID, to realize a demonstrator of a dry SMES device in order to validate the functions to support the distribution grid.

The compensator and the different control strategies have been presented. The comparison showed that the close loop without harmonic compensation had the best performance. Two current limitation control strategies for the inverter were implemented: a “hardware” fast limitation and a “software” slow limitation. For each limitation, it has been presented the control structure and the simulative results focusing on their effects. A protection strategy for internal faults, based on a residual current relay, has been shown. To test the relay performances as suitable solution for the fault detection, different faults have been simulated and the results confirm the good approach.

Future developments will be the best definition of the intervention threshold and timing values of the supervisor system in order to avoid unintentionally trip and load damage. Furthermore, for the prosecution of the DRYSMES4GRID project, Control Hardware in the Loop (CHIL) Real Time simulations will be developed for testing the control logics.

Acknowledgment

This work has been financed by the Research Fund “B” for the Italian Electrical System under the Contract Agreement between DRYSMES4GRID partners and the Ministry of Economic Development - General Directorate for Nuclear Energy, Renewable Energy and Energy Efficiency in compliance with the Decree of March 8, 2006.

References

[1] J. Milanovic e M. Negnevitsky, “Power Quality problems and solutions: current understanding” in 8th International Conference on Harmonics and Quality of Power. Proceedings (Cat. No.98EX227), Athens, Greece, 1998.

[2] C. Gandolfi, R. Chiumeo, D. Raggini, R. Faranda, A. Morandi, R. Ferdeghini, M. Tropeano e S. Turtù, “Study of a Universal Power SMES Compensatore for LV distribution Grid”, in 2018 AEIT International Annual Conference, 2018.

[3] D. Raggini, “Study of a SMES interface device for electrical LV distribution grid”, *Master thesis*, Politecnico di Milano, July 2018.

[4] D. Gargantini, “Strategie di controllo e di limitazione per un dispositivo elettronico di compensazione”, *Master thesis*, Politecnico di Milano, April 2019 (italian language).

[5] F. Belloni, R. Chiumeo, C. Gandolfi and S. Pugliese, “A Universal Compensator for Power Quality Improvement in LV Distribution Grids,” in CIRED 2015, 15-18 June 2015.

[6] F. Belloni, R. Chiumeo, C. Gandolfi and A. Villa, “Performance test of a PQ Universal Compensator through Control Hardware In the Loop simulation, in ICCEP 2017, Santa Margherita Ligure, Giugno 2017.

[7] N. Bottrell e T. C.Green, “Comparison of current-limiting strategies during fault ride-through of inverters to prevent latch-up and wind-up,” in IEEE Transactions on Power Electronics, 2014.

[8] C. A.Plet, M. Brucoli, J. McDonald e T. C.Green, “Fault models of inverter-interfaced distributed generators: experimental verification and application to fault analysis, ” in 2011 IEEE Power and Energy Society General Meeting, 2011.

[9] C. Gandolfi, R. Chiumeo, A. Clerici, D.Gargantini, D. Raggini, “Rapporto tecnico contenente i principali risultati degli studi digitali e i requisiti per l’interfacciamento delle schede di controllo al simulatore Real Time”, RSE report for DRY4SMES, 2020 (italian language).